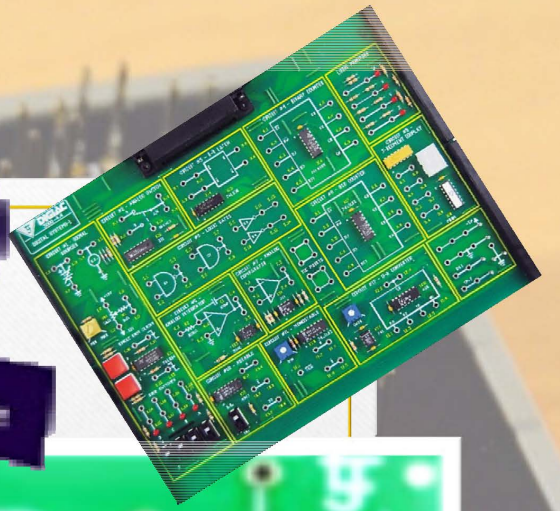


ELECTRONICS II

Lecture No.(15)- Semester 2

Assist.Prof.Dr. HASSAN M. JABER Al-TA'II
Faculty of Science
Al-Muthanna University

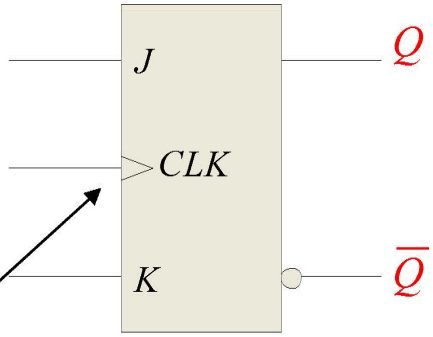
2018-2019

Summary

Flip-flops

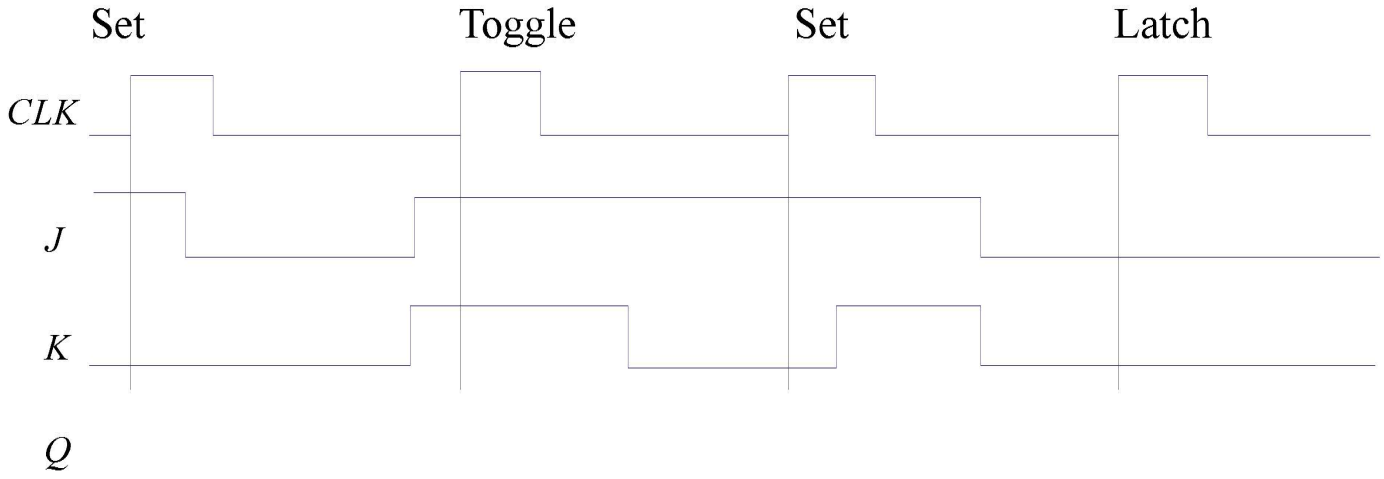
Example

Determine the Q output for the J-K flip-flop, given the inputs shown.



Notice that the outputs change on the leading edge of the clock.

Solution

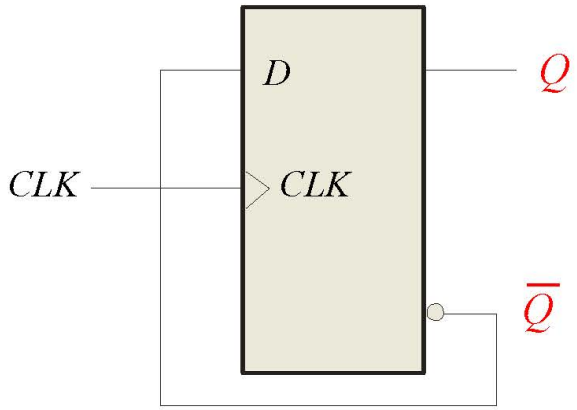


Summary

Flip-flops

A D-flip-flop does not have a toggle mode like the J-K flip-flop, but you can hardwire a toggle mode by connecting $\overline{Q}$ back to D as shown. This is useful in some counters as you will see in Chapter 8.

For example, if Q is LOW, $\overline{Q}$ is HIGH and the flip-flop will toggle on the next clock edge. Because the flip-flop only changes on the active edge, the output will only change once for each clock pulse.



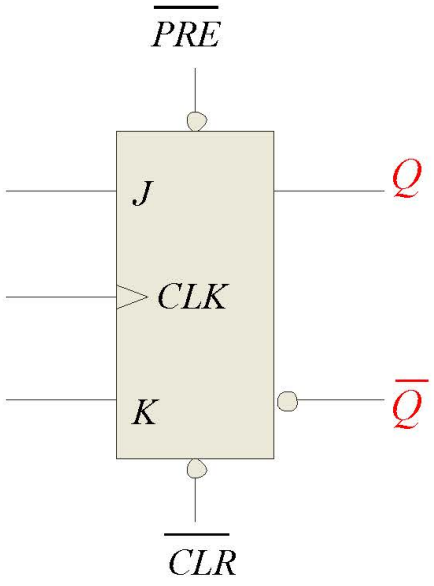
D flip-flop hardwired for a toggle mode

Summary

Flip-flops

Synchronous inputs are transferred in the triggering edge of the clock (for example the *D* or *J-K* inputs). Most flip-flops have other inputs that are *asynchronous*, meaning they affect the output independent of the clock.

Two such inputs are normally labeled preset (*PRE*) and clear (*CLR*). These inputs are usually active LOW. A J-K flip flop with active LOW preset and CLR is shown.

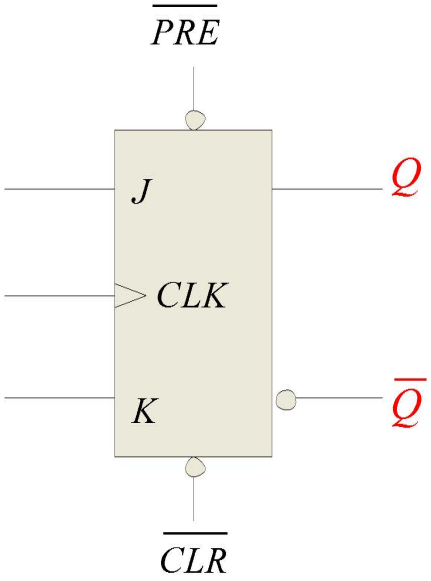


Summary

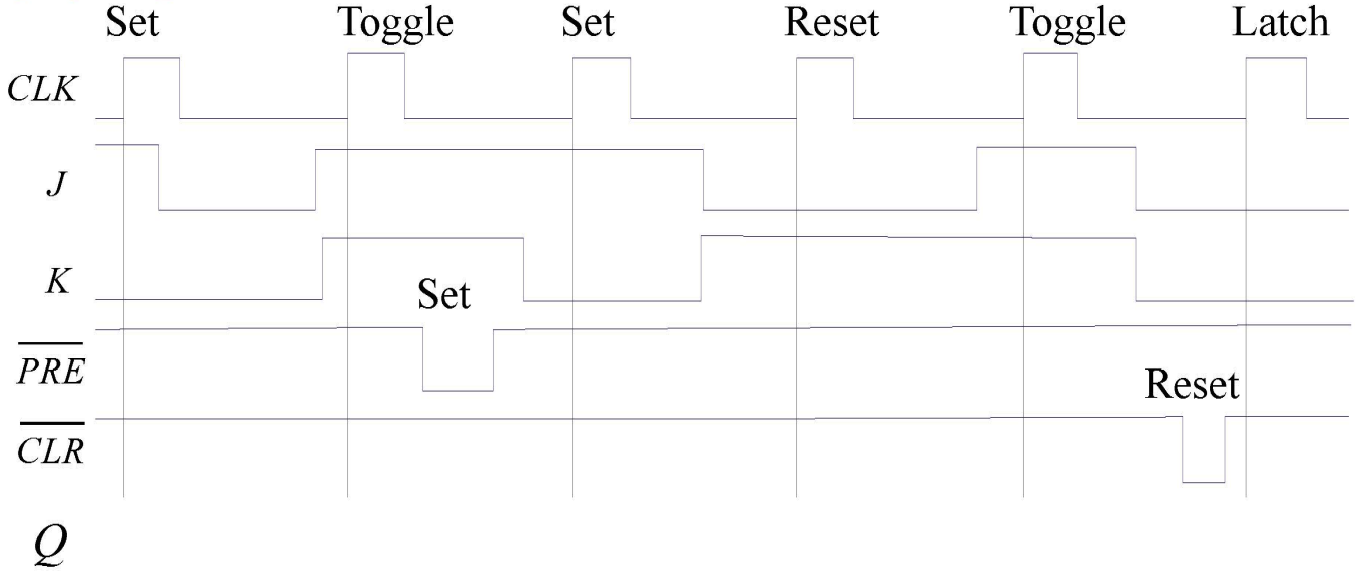
Flip-flops

Example

Determine the Q output for the J-K flip-flop, given the inputs shown.



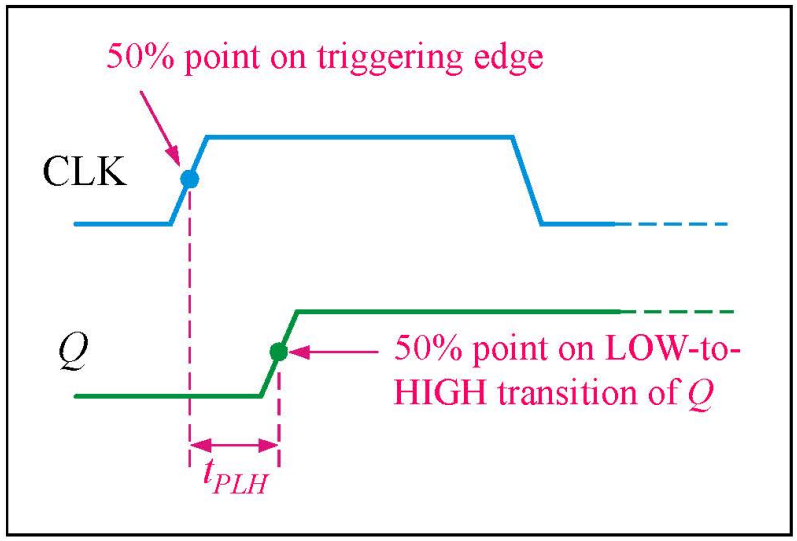
Solution



Summary

Flip-flop Characteristics

Propagation delay time is specified for the rising and falling outputs. It is measured between the 50% level of the clock to the 50% level of the output transition.

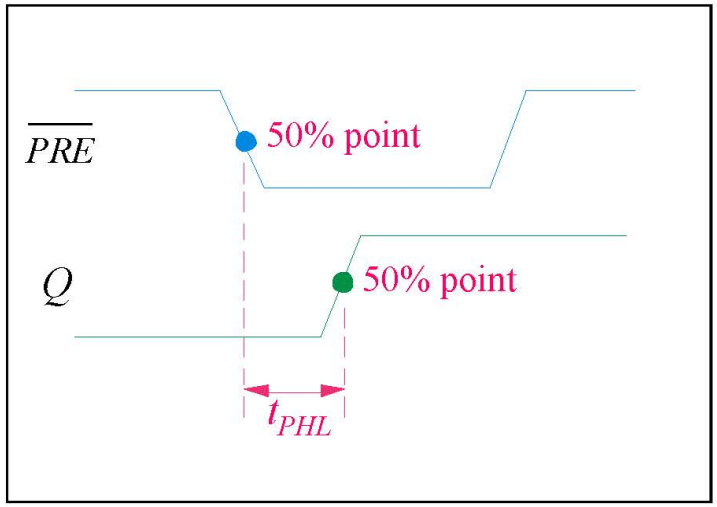


The typical propagation delay time for the 74AHC family (CMOS) is 4 ns. Even faster logic is available for specialized applications.

Summary

Flip-flop Characteristics

Another **propagation delay time** specification is the time required for an *asynchronous* input to cause a change in the output. Again it is measured from the 50% levels. The 74AHC family has specified delay times under 5 ns.

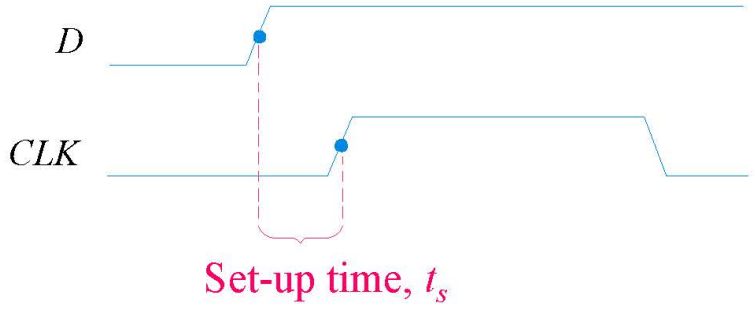


Summary

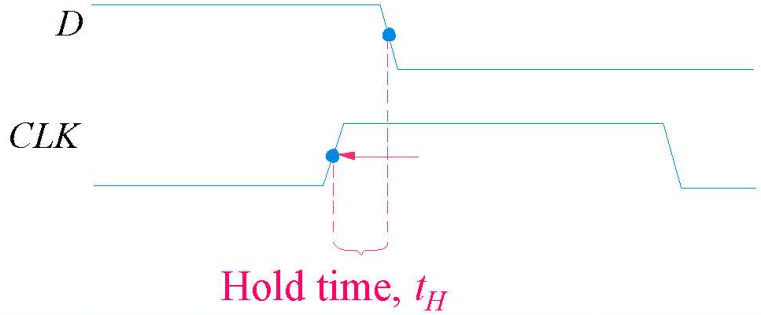
Flip-flop Characteristics

Set-up time and **hold time** are times required before and after the clock transition that data must be present to be reliably clocked into the flip-flop.

Setup time is the minimum time for the data to be present *before* the clock.



Hold time is the minimum time for the data to *remain* after the clock.



Summary

Flip-flop Characteristics

Other specifications include maximum clock frequency, minimum pulse widths for various inputs, and power dissipation. The power dissipation is the product of the supply voltage and the average current required.

A useful comparison between logic families is the **speed-power product** which uses two of the specifications discussed: the average propagation delay and the average power dissipation. The unit is energy.

Example What is the speed-power product for 74AHC74A? Use the data from Table 7-5 to determine the answer.

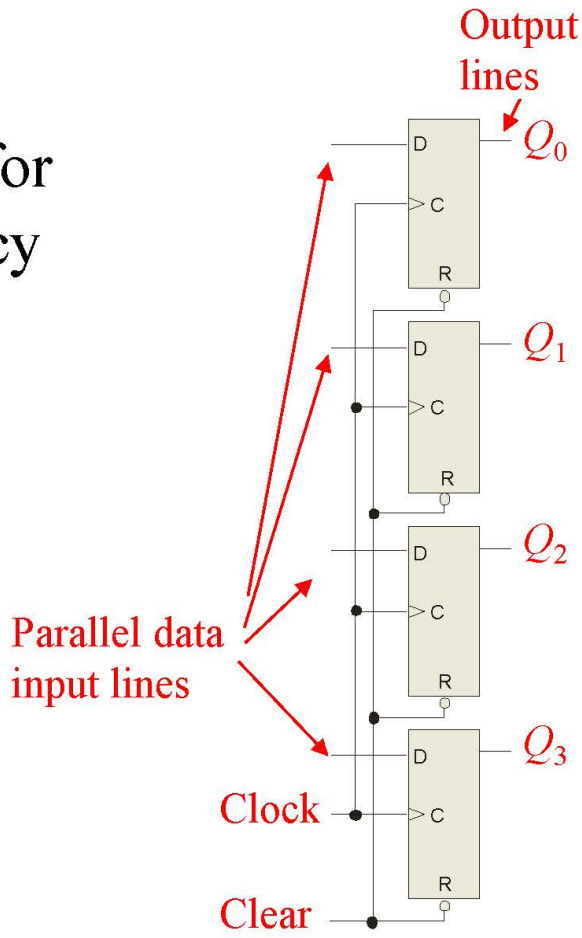
Solution From Table 7-5, the average propagation delay is 4.6 ns. The quiescent power dissipated is 1.1 mW. Therefore, the speed-power product is 5 pJ

Summary

Flip-flop Applications

Principal flip-flop applications are for temporary data storage, as frequency dividers, and in counters.

Typically, for **data storage** applications, a group of flip-flops are connected to parallel data lines and clocked together. Data is stored until the next clock pulse.

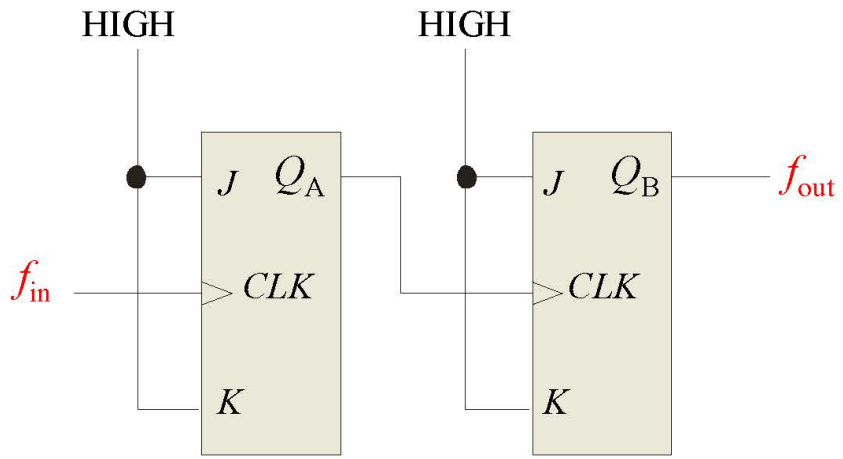


Summary

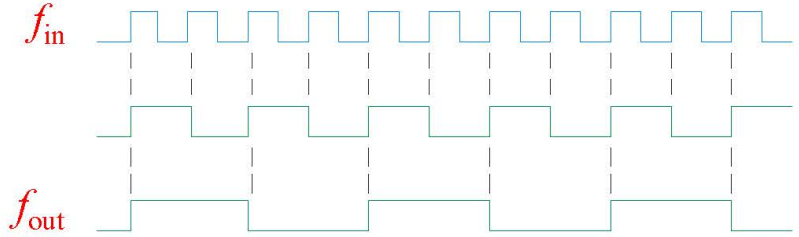
Flip-flop Applications

For **frequency division**, it is simple to use a flip-flop in the toggle mode or to chain a series of toggle flip flops to continue to divide by two.

One flip-flop will divide f_{in} by 2, two flip-flops will divide f_{in} by 4 (and so on). A side benefit of frequency division is that the output has an exact 50% duty cycle.



Waveforms:

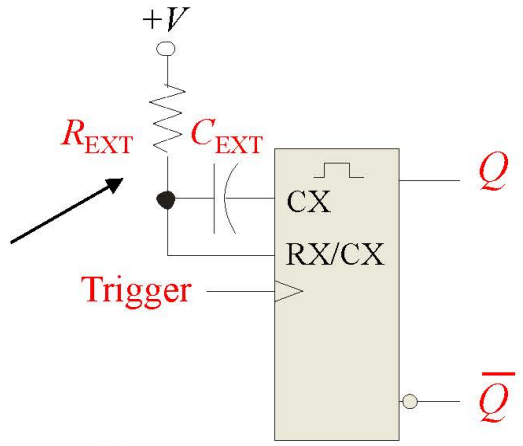


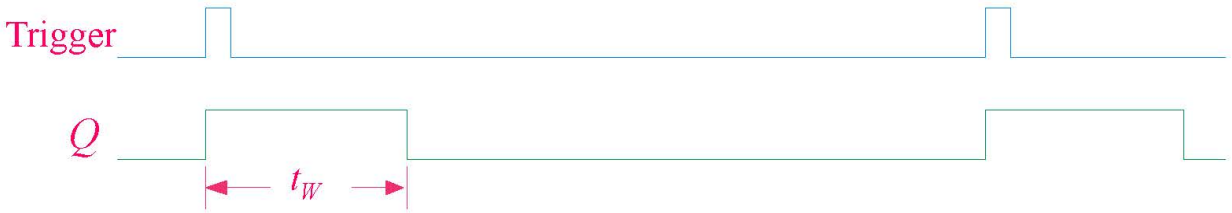
Summary

One-Shots

The **one-shot** or **monostable** multivibrator is a device with only one stable state. When triggered, it goes to its unstable state for a predetermined length of time, then returns to its stable state.

For most one-shots, the length of time in the unstable state (t_W) is determined by an external *RC* circuit.





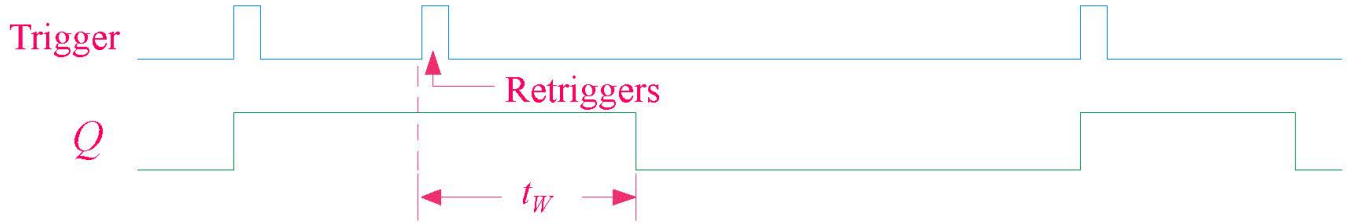
Summary

One-Shots

Nonretriggerable one-shots do not respond to any triggers that occur during the unstable state.

Retriggerable one-shots respond to any trigger, even if it occurs in the unstable state. If it occurs during the unstable state, the state is extended by an amount equal to the pulse width.

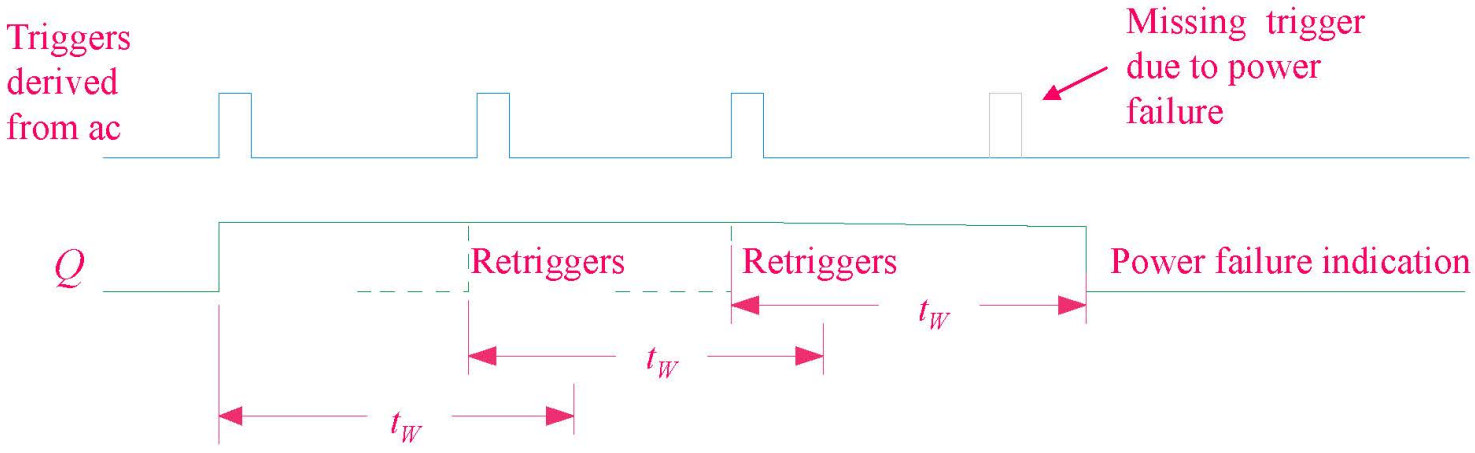
Retriggerable one-shot:



Summary

One-Shots

An application for a retriggerable one-shot is a power failure detection circuit. Triggers are derived from the ac power source, and continue to retrigger the one shot. In the event of a power failure, the one-shot is not triggered and an alarm can be initiated.

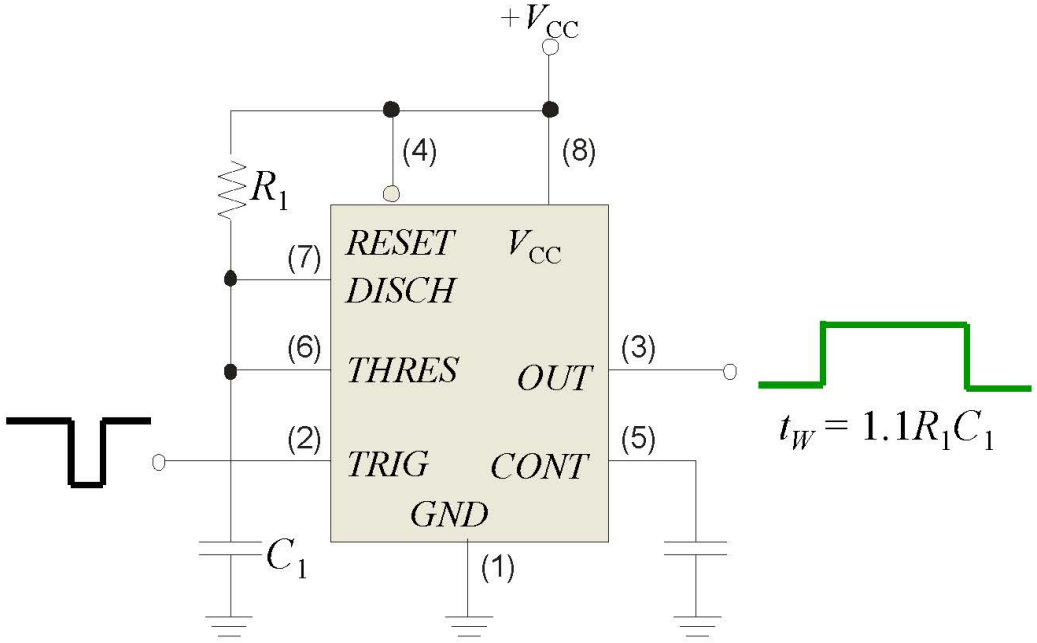


Summary

The 555 timer

The 555 timer can be configured in various ways, including as a one-shot. A basic one shot is shown. The pulse width is determined by R_1C_1 and is approximately $t_W = 1.1R_1C_1$.

The trigger is a negative-going pulse.

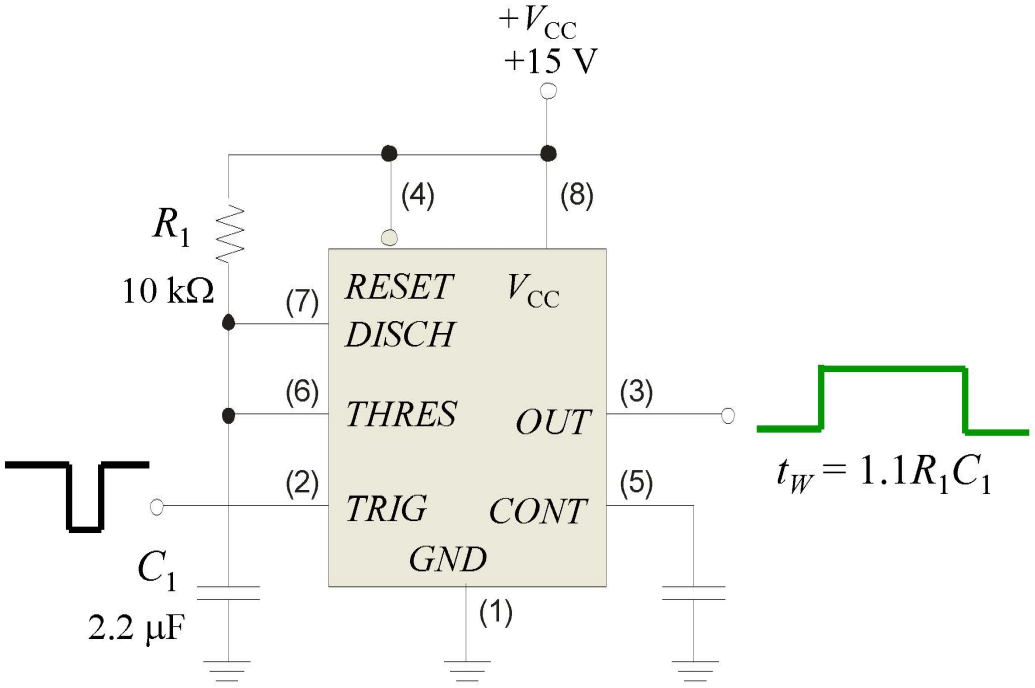


Summary

The 555 timer

Example Determine the pulse width for the circuit shown.

Solution $t_W = 1.1R_1C_1 = 1.1(10\ \text{k}\Omega)(2.2\ \mu\text{F}) = 24.2\ \text{ms}$



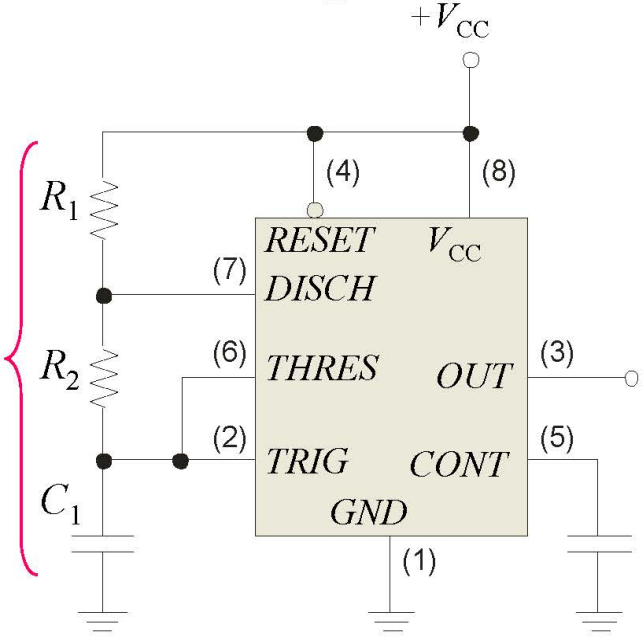
Summary

The 555 timer

The 555 can be configured as a basic astable multivibrator with the circuit shown. In this circuit C_1 charges through R_1 and R_2 and discharges through only R_2. The output frequency is given by:

$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

The frequency and duty cycle are set by these components.



Summary

The 555 timer

Given the components, you can read the frequency from the chart. Alternatively, you can use the chart to pick components for a desired frequency.